



## Design and Strategy for Reliability in ICs

### Title—Design and Strategy for Reliability in ICs

#### Presenter

Stephen Meats

#### Date

2—4 June 2009  
iSLI Livingston

#### Cost

£1,050 per person + VAT

*(Discounts available please enquire)*

Mentor Graphics Passbook = 3 Tokens

#### Contact

If you have any course queries, please contact Suzanne O'Hare on 01506 469303 or by emailing [suzanne.ohare@sl-i-institute.ac.uk](mailto:suzanne.ohare@sl-i-institute.ac.uk).

#### Course Aims

This course demonstrates the importance of Reliability throughout the whole product creation process from the design phase through to issues with the end product. A "right first time" approach to Reliability results in reduced engineering costs and an improved time to market. This can be achieved by having a clear Reliability Strategy from the outset with an emphasis on Design for Reliability and Design for Analysis.

#### Who Should Attend

- Designers involved in IC or Library Design
- Reliability Engineers
- Failure Analysis Engineers
- Test Engineers
- Students of Electronic Engineering at MSC Level

The course is relevant to a wide range of disciplines, and adds value to those with a Reliability background by exploring the relationships between Reliability, Design and Failure Analysis.

### Course Content

#### Day 1—Introduction / Reliability Qualifications

- What is a Reliability?
- How do we implement it?
- Importance of "DfX" (DfR / DfT/ DfA)
- Overview of Failure Modes: Early/Life Intrinsic Life/End of Life Failures
- What is a Reliability Strategy?
- Integration of Reliability throughout the whole product development cycle
- Reliability Requirements for different markets
- PPM, FPM, FITs
- Statics, the significance of sample sizes
- How to define a programme of stress tests based on commercial market, similarity to existing designs, and other available data
- Process qualifications
- Package qualifications
- Use of test chips
- Use of third party reliability operations
- Hardware design for reliability: HTOL, HAST, ESD etc.
- Test program requirements for Reliability
- Interpretation of ATE test results
- How to interpret life test failures
- The Role of FA in Reliability Qualifications

#### Day 2—Design for Reliability

- Overview of DfR / DfA
- How other functions can help: Reliability, Test, FA Engineers
- Principles of Best Practice in DfR (Design for Reliability)
- Risk Analysis in design
- Use of Historical Data

#### ESD

- Explanation of Human Body Model, Machine Model, Charged Device Model
- Supply Protection

- On chip ESD protection
- Chip protection using Standard Cell Libraries
- Pad based ESD Protection
- Rail Based ESD protection
- Rail Clamp Networks
- Influence of layout/positioning of cells on ESD protection

#### Checking an IC Design for Good ESD Performance

- Developing and applying ESD guidelines for design

#### Other DfR Issues

- Latch Up
- Hot Electron
- NBTI
- Electromigration
- Developing and applying guidelines for the above

#### The Future of DfR

- Nanometer CMOS ICs
- The Effects of Scaling of IC Design on IC Reliability
- Effect of gate oxide thickness, smaller metal tracks, high k dielectrics
- Impact of scaling on debug and FA

### **Day 3—Design for Analysis / Principles of Failure Analysis**

#### Design for Analysis

- Principles of Best Practice in DfA (Design for Analysis)
- Power supply configuration
- Use of JTAG controller
- Navigation markers
- Memory Mapping
- Use of scan testable logic
- Electrical diagnostics
- Interface between blocks
- DfA Pads issues
- DfA Memory issues
- Choice of package
- Importance of back side access
- Interface of package to analysis hardware
- Involvement of FA in design process

#### Principles of Failure analysis

- The FA 'mindset' and its relationship to DfA
- Field Failures vs. Qualification Failures
- Package and assembly issues
- Wafer fabrication issues
- Design issues
- Revisit risk register / known design issues
- Electrical analysis / diagnosis
- Use of schematic / layout in fault location
- Use of FIB circuit edits

#### Physical techniques for fault location

- LXTAL / PEM / OBIRCH / Laser Scan / Optical Timing
- Hardware interfaces for Failure Analysis
- Back side techniques
- Use of FIB as an FA tool
- Feedback of FA to design
- New challenges for FA

#### **Presenter**

Stephen Meats has 25 years experience of Electronics Reliability, in diverse technologies ranging from printed circuit board materials to the latest deep submicron IC technologies. Involvement with a wide range of markets including Automotive, Military, and Space has given an insight into Reliability issues across the whole Electronics Industry. Active participation in symposia such as NMI's Failure Analysis and Characterisation meeting sparked a keen interest in imparting his skills and knowledge to others.

#### **Fees**

Fees cover tuition, course notes, lunches and light refreshments.

#### **Accommodation**

Information on local hotels is available from Amanda Connelly [amanda.connelly@sli-institute.ac.uk](mailto:amanda.connelly@sli-institute.ac.uk).

#### **Cancellations**

A 10% administration fee is levied for cancellations made up to two weeks prior to the start of the course. Cancellations thereafter will be liable to the loss of the full fee. Substitutions may be made at any time up until the start of the course.

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